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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/716,907

11/19/2003

Laura Pozzi

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EXAMINER

MITCHELL, JASON D

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/716,907	Applicant(s) POZZI ET AL.	
	Examiner Jason Mitchell	Art Unit 2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 November 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 15-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 15-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This action is in response to a request for continued examination filed on 11/20/08.

Claims 15-21 are pending in this application.

Response to Arguments

Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 19 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "near-optimal" in claim 19 is a relative term which renders the claim indefinite. The term "near-optimal" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Note that for the purposes of this examination claim 19 will be treated in conjunction with claim 18 which only recites "optimal".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 15-21 are rejected under 35 U.S.C. 102(a)¹ as being anticipated by “Automatic Application-Specific Instruction-Set Extensions under Microarchitectural Constraints” by Verma, Atasu, Vuletic, Pozzi and lenne. (Verma).

Regarding Claims 15 and 21: Verma disclose a process for generating a micro-processor instruction set extension for a processor application, comprising:

generating a data flow graph $G(V,E)$ of nodes V representing primitive operations of the processor application and edges E representing data dependencies of said application (see pg. 2, Section 4. 1st par. “ $G(V,E)$ the DAG representing the dataflow of a basic block, the nodes V represent primitive operations and the edges E represent data dependencies”);

evaluating subgraphs S of $G(V,E)$ as candidates for an instruction set extension, each said subgraph S having a number of inputs $IN(S)$ (pg. 3, col. 1, 2nd full par. “ $IN(S)$

¹ The examiner notes that the conference at which this reference was presented was held on 11/19/02, exactly 1 year before the application was filed. Accordingly in the instant action the reference is applied under 35 USC 102(a), however if this document was made publicly available prior to the conference (e.g. provided to attendees in some sort of 'materials' package) the reference would represent a 102(b) statutory bar. Regardless, given the different inventive entities the point is moot and is merely mentioned here for the sake of completeness.

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the number of predecessor nodes of those edges which enter the cut S ") and a number of outputs $OUT(S)$ (pg. 3, col. 1, 2nd full par. " $OUT(S)$ is the number of predecessor nodes in S of edges exiting the cut S "), said instruction set extension having a number of available register-file read ports N_{in} and a number of available register-file write ports N_{out} (pg. 3, col. 1, last par. " N_{in} and N_{out} indicate the register-file read and write ports, respectively");

wherein said evaluating a subgraph S includes,

if $OUT(S)$ is less than or equal to N_{out} , and if S is convex, and if $IN(S)$ is less than or equal to N_{in} , then identifying S as a candidate for transformation into an instruction set extension, else disregarding S as a candidate for transformation into an instruction set extension (see pg. 3, col. 1, statement of Problem 1 "find the cut S which maximizes $M(S)$ under the following constraints: 1 $IN(S) \leq N_{in}$, 2. $OUT(S) \leq N_{out}$, and 3. S is convex");

wherein S is convex when no path exists from a node in S to another node in S when said path involves a node that is not in S (pg. 3, col. 1, 3rd full par. "we call the cut S convex if there exists no path from a node u [in the set] S to another node v [in the set] S which involves a node w [not in the set] S ");

evaluating said identified candidates using a function $M(S)$ as a measure of merit (see pg. 3, col. 1, statement of Problem 1 "find the cut S which maximizes $M(S)$ ");

transforming said instruction set by adding an instruction set extension representing said identified candidate to said instruction set if said candidate satisfies

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said function $M(S)$ (pg. 1, col. 2, 1st full par. “generate the required instruction–set extensions”).

Regarding Claim 16: The rejection of claim 15 is incorporated; further Verma discloses:

performing said evaluating of subgraphs S for a plurality all subgraphs S in a plurality of data flow graphs G representing all basic blocks of said processor application (pg. 5, section 7, 1st par. “Application C-code is compiled ... and the dataflow graphs are processed by our algorithm”);

selecting a number j of identified candidates satisfying said evaluation to form a candidate set S_j which maximizes $\sum_j M(S_j)$ (Abstract “selects maximal-speedup convex subgraphs of the application dataflow graph”; Note the plurality of subgraphs. Because of the nature of the calculations involved this maximal set will necessarily maximize $\sum_j M(S_j)$); and

transforming said candidate set S_j into an instruction set extensions for said processor application (pg. 1, col. 2, 1st full par. “generate the required instruction–set extensions”; Again note the plurality of extensions).

Regarding Claim 17: The rejection of claim 15 is incorporated; further Verma discloses:

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performing said evaluation of subgraphs S for a plurality of subgraphs S in a single basic block of said processor operation (pg. 3, col. 1, 1st full par. A cut S is a subgraph of G ");

identifying a single optimal S in said plurality according to said function $M(S)$ (see pg. 3, col. 1, statement of Problem 1 "find the cut S which maximizes $M(S)$ under the following constraints: 1 $IN(S) \leq N_{in}$, 2. $OUT(S) \leq N_{out}$, and 3. S is conve[x]"); and

transforming said instruction set by adding an instruction set extension representing only said optimal S (pg. 1, col. 2, 1st full par. "generate the required instruction-set extensions").

Regarding Claim 20: The rejection of claim 17 is incorporated; further Verma discloses:

performing a topological sort on G (pg. 3, section 5 2nd par. "starts with a topological sort on G ");

ordering nodes of G such that if G contains and edge (u,v) then u appears after v in said ordering (pg. 3, section 5 2nd par. "Nodes of G are ordered such that if G contains an edge (u,v) then u appears after v in the ordering"); and

utilizing a recursive search function based on said ordering (pg. 3, section 5 2nd par. "The algorithm uses a recursive search").

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over “Automatic Application-Specific Instruction-Set Extensions under Microarchitectural Constraints” by Verma, Atasu, Vuletic, Pozzi and lenne. (Verma) in view of “Automatic Topology-Based Identification of Instruction-Set Extensions for Embedded Processors” by Pozzi, Vuletic, and lenne (Pozzi).

Regarding Claims 18 and 19: The rejection of claim 17 is incorporated; further Verma discloses:

identifying an optimal set of subgraphs S in a plurality of basic blocks of said processor operation according to said function M(S) (Abstract “selects maximal-speedup convex subgraphs of the application dataflow graph”; Note the plurality of subgraphs); and

transforming said instruction set by adding one or more instruction set extensions representing said optimal set of non-overlapping subgraphs (pg. 1, col. 2, 1st full par. “generate the required instruction–set extensions”).

Verma does not appear to explicitly disclose the detected set consists of non-overlapping subgraphs. *(It is noted, however, that Verma appears to use the same identification techniques and thus would seem to detect the same sets. For example compare Verma's figs. 4-5 and the applicants' figs. Figs. 4-5. Regardless the limitation is addressed through combination in an effort to expedite prosecution.)*

Pozzi teaches identifying an optimal set of non-overlapping subgraphs S in a plurality of basic blocks (Pozzi pg. 6, section 5, 1st par. "partition automatically the data flow graph of an application ... in disjoint subgraphs which are maximal under the constraint")

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include only non-overlapping subgraphs, as taught by Pozzi (pg. 6, section 5, 1st par. "disjoint subgraphs"), in the optimal set of subgraphs identified in Verma (Abstract "maximal-speedup convex subgraphs"). It would have been obvious to one of ordinary skill in the art at the time the invention was made do so because Pozzi discloses an efficient algorithm to partition automatically the data flow graph of an application" (pg. 6, section 5, 1st par.)

Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Automatic Application-Specific Instruction-Set Extensions under Microarchitectural Constraints" by Verma, Atasu, Vuletic, Pozzi and lenne.

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(Verma) in view of “Automatic Application-Specific Instruction-Set Extensions under Microarchitectural Constraints” by Atasu, Pozzi and lenne (Atasu).

Regarding Claims 18 and 19: The rejection of claim 17 is incorporated; further Verma discloses:

identifying an optimal set of subgraphs S in a plurality of basic blocks of said processor operation according to said function M(S) (Abstract “selects maximal-speedup convex subgraphs of the application dataflow graph”; Note the plurality of subgraphs); and

transforming said instruction set by adding one or more instruction set extensions representing said optimal set of non-overlapping subgraphs (pg. 1, col. 2, 1st full par. “generate the required instruction–set extensions”).

Verma does not appear to explicitly disclose the detected set consists of non-overlapping subgraphs. *(It is noted, however, that Verma appears to use the same identification techniques and thus would seem to detect the same sets. For example compare Verma’s figs. 4-5 and the applicants’ figs. Figs. 4-5. Regardless the limitation is addressed through combination in an effort to expedite prosecution.)*

Atasu teaches identifying an optimal set of non-overlapping subgraphs S in a plurality of basic blocks (pg. 3, section 5, 1st par. “(2) find an optimal set of nonoverlapping cuts in several basic blocks”).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include only non-overlapping subgraphs, as taught by Atasu (pg. 3, section 5, 1st par. "optimal set of nonoverlapping cuts"), in the optimal set of subgraphs identified in Verma (Abstract "maximal-speedup convex subgraphs"). It would have been obvious to one of ordinary skill in the art at the time the invention was made to do so because Atasu discloses a "more general algorithm which selects maximal-speedup convex subgraphs of the application" (Atasu Abstract).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Mitchell whose telephone number is (571)272-3728. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bullock Lewis can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason Mitchell/
Examiner, Art Unit 2193